UNIVERSITY of GUELPH

CIS*3120: Digital Systems I

Bonus

Date: Monday, April 1 **Offering**: Winter 2019

This assignment is due at the beginning of class, Monday, April 5. If you have any questions, please see the instructor or the teaching assistant for clarification. Answer all questions in the spaces provided. Remember to *neatly print your name* along with your *student ID* below. Loose (i.e., unstapled) sheets will not be accepted. Thank you!

Name: _____ Student ID: _____

Question	Mark
1 (4)	
2 (8)	
3 (8)	
Total (20)	

1. (**Memory Parameters)** The memory units that follow are specified by the number of words times the number bits per word. How many address lines and input-output data lines are needed in each case?

   a. 8K x 32

   b. 2G x 8

   c. 16M x 32

   d. 256K x 64

2. (**Coincident Decoding)** A 16K x 4 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.

    a. What is the size of each decoder, and how many AND gates are required for decoding the address?

    b. Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6000.

3. (**Memory Design)** How many 32K x 8 SRAM chips are needed to provide a memory capacity of 256K bytes?

    a. How many of the lines of the address must be used to access 256K bytes?

    b. How many of these lines are connected to the address inputs of all chips?

    c. How many lines must be decoded for the chip select inputs?

    d. Specify the size of the decoder.